
FULL LAYER-III ISO/IEC 11172-3 AUDIO DECODER

- Single-chip ISO/IEC 11172-3 Layer III Audio Decoder
 - Supports All MPEG Bit Rates Including Free Format
 - Supports 32/44.1/48KHz Sampling Frequencies for MPEG Bit Stream
 - Supports Single Channel, Dual Channel, Stereo, and Joint Stereo
 - Any Combination of Intensity Stereo and MS Stereo is supported.
 - Serial Bit Stream Input
 - 8-bit Host Interface Port
 - Digital Volume Control
 - Digital Bass/Treble Control
 - 6 Band Equalizer Function
 - Voice Record/Playback Capability
 - Voice Monitoring Capability
 - On-chip DAC with 1-bit Sigma Delta Modulation
 - Supports Off-chip DAC Interface
 - On-chip ADC with 12-bit Resolution
 - Power Management to Reduce Power Consumption
 - PLL for Internal Clocks and for Output PCM Clock Generation
 - Single 16.9344MHz External Clock Input
 - 2.7 V Operation
 - Small Footprint 64-pin Thin Quad Flat Package
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DESCRIPTION

TL7232MD is a single-chip ISO/IEC 11172-3 Layer III audio decoder, capable of decoding compressed elementary bit streams as specified in ISO/IEC standard. Since it integrated on-chip ADC and on-chip DAC, it can provide you more small and cheaper solution for MP3 player application. It is designed to be well suited for portable audio appliances.

TL7232MD receives the input data bit stream through a serial data interface. The decoded signal is 16-bit serial PCM format that can be sent directly to DAC. The generated PCM data can be sent to on-chip DAC or off-chip DAC according to user preference. The off-chip DAC interface is programmable to adapt the PCM output of TL7232MD to the most common DACs used on the market.

An 8-bit host interface port is provided to receive control information from and send status information to host. 8-bit microcontrollers such as those of Intel or Motorola can be connected easily.

TL7232MD has the capability of compressing voice signals. It can receive voice signals through on-chip ADC. The compressed voice signals are transmitted to or received from host through serial data interface. It can also reproduce the voice signals from the compressed voice signals.

FUNCTIONAL BLOCK DIAGRAM

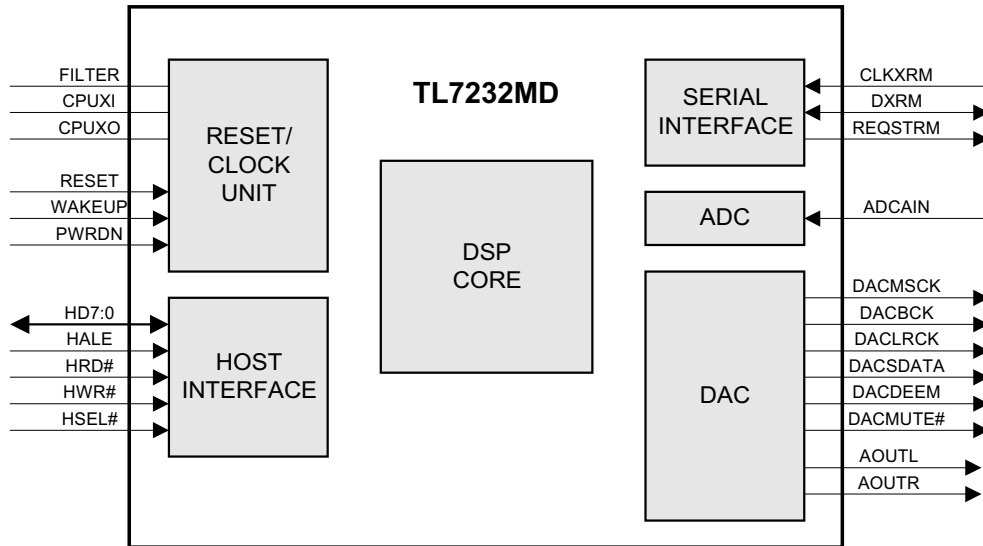


Figure 1. Functional Block Diagram of TL7232MD

PIN DESCRIPTION

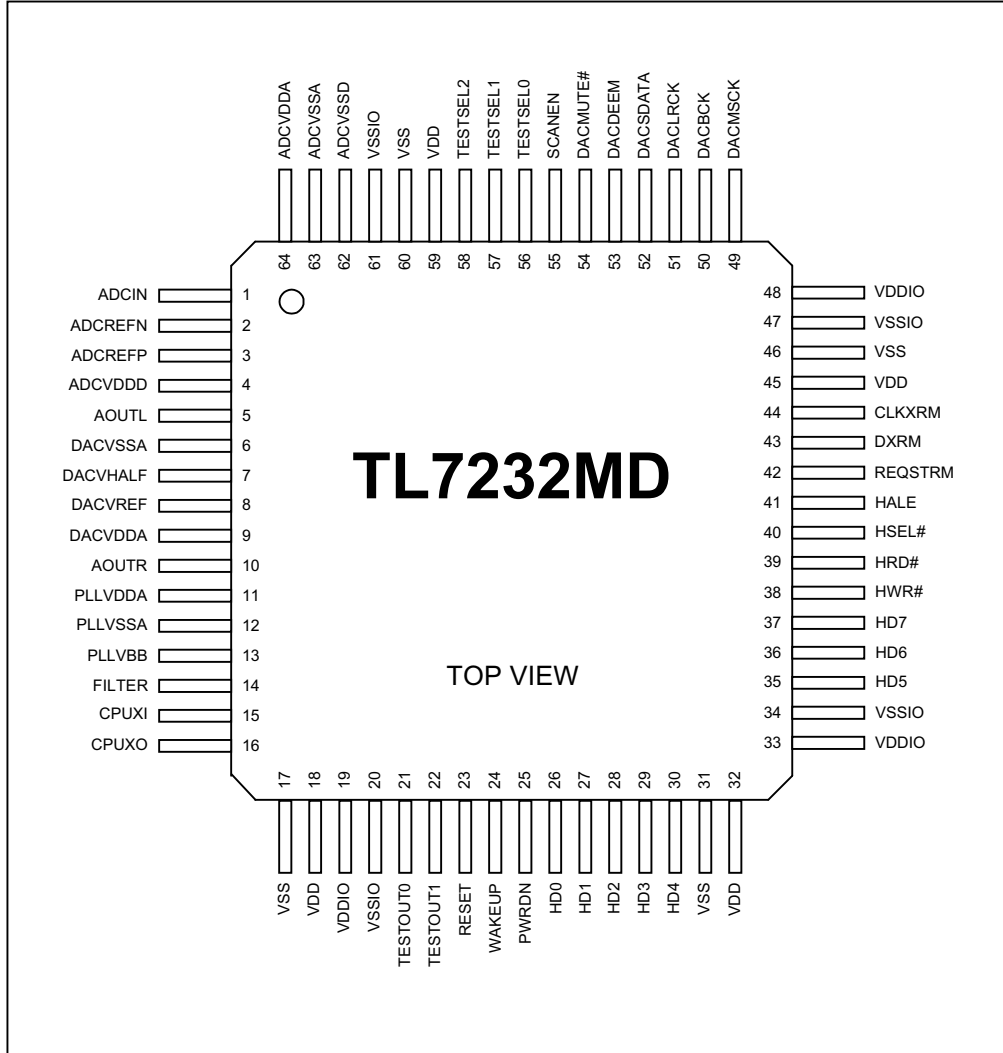


Figure 2. 64-pin Thin Quad Flat Package (TQFP)

Table 1. Pin Locations with Pin Names

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	ADCAIN	17	VSS	33	VDDIO	49	DACMSCK
2	ADCREFN	18	VDD	34	VSSIO	50	DACBCK
3	ADCREFP	19	VDDIO	35	HD5	51	DACLRCK
4	ADCVDDD	20	VSSIO	36	HD6	52	DACS DATA
5	AOUTL	21	TESTOUT0	37	HD7	53	DACDEEM
6	DACVSSA	22	TESTOUT1	38	HWR#	54	DACMUTE#
7	DACVHALF	23	RESET	39	HRD#	55	SCANEN
8	DACVREF	24	WAKEUP	40	HSEL#	56	TESTSEL0
9	DACVDDA	25	PWRDN	41	HALE	57	TESTSEL1
10	AOUTR	26	HD0	42	REQSTRM	58	TESTSEL2
11	PLLVDDA	27	HD1	43	DXRM	59	VDD
12	PLLVSSA	28	HD2	44	CLKXRM	60	VSS
13	PLLVB	29	HD3	45	VDD	61	VSSIO
14	FILTER	30	HD4	46	VSS	62	ADCVSSD
15	CPUXI	31	VSS	47	VSSIO	63	ADCVSSA
16	CPUXO	32	VDD	48	VDDIO	64	ADCVDDA

Table 2. Pin Functions with Location

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
ADCAIN	1	DACMUTE#	54	HALE	41	VDD	18
ADCREFN	2	DACS DATA	52	HRD#	39	VDD	32
ADCREFP	3	DACVHALF	7	HSEL#	40	VDD	45
ADCVDDA	64	DACVREF	8	HWR#	38	VDD	59
ADCVDDD	4	DACVSSA	6	PLLVB	13	VDDIO	19
ADCVSSA	63	DACVDDA	9	PLLVDDA	11	VDDIO	33
ADCVSSD	62	DXRM	43	PLLVSSA	12	VDDIO	48
AOUTL	5	FILTER	14	PWRDN	25	VSS	17
AOUTR	10	HD0	26	REQSTRM	42	VSS	31
CLKXRM	44	HD1	27	RESET	23	VSS	46
CPUXI	15	HD2	28	SCANEN	55	VSS	60
CPUXO	16	HD3	29	TESTOUT0	21	VSSIO	20
DACBCK	50	HD4	30	TESTOUT1	22	VSSIO	34
DACDEEM	53	HD5	35	TESTSEL0	56	VSSIO	47
DACLRCK	51	HD6	36	TESTSEL1	57	VSSIO	61
DACMSCK	49	HD7	37	TESTSEL2	58	WAKEUP	24

Table 3. Pin Descriptions

Signal Name	Type	Description
Internal PLL Interface		
CPUXI	I	CPU Clock In. 16.9344MHz crystal clock input.
CPUXO	O	CPU Clock Out. 16.9344MHz crystal clock output.
FILTER	O	Charge Pump Out. External capacitor should be connected between this pin and analog ground.
Reset & Power Down Control		
RESET	I	Chip Reset. Reset input to the chip. Internal pull down.
WAKEUP	I	Wake Up. When high, chip is waked up from SLEEP state. This pin should be remained active at least 1 clock cycle and inactive before the host issues next SLEEP command. Internal pull down.
PWRDN	I	Power Down. This pin controls PWRDOWN state. When high, chip goes to very low power consumption state. After deactivation, WAKEUP pin should be remained low at least 150 μ s. Internal pull down. (Restriction: This pin should be active ONLY in SLEEP state. Otherwise, Chip reset should be activated.)
MCU Serial Interface		
CLKXRM	I	Serial Clock. MCU serial interface clock.
DXRM	I/O	Serial Data. When MCU transmits data, this data pin is sampled at negative edge of CLKXRM. When MCU receives data, Data is valid from negative edge of CLKXRM to next negative edge of CLKXRM. DXRM should be sampled at positive edge of CLKXRM. After reset, TL7232MD is set to transmit the most significant bit first.
REQSTRM	O	Request Bit Stream Data. MCU must check this pin to determine to continue receiving or transmitting. MCU should transmit or receive data during this signal active.
MCU HIP(Host Interface Port) Interface		
HSEL#	I	HIP Enable. When Low, HIP is selected.
HALE	I	HIP Address Latch Enable. When High, HD7:0 should have HIP address, which is sampled at negative edge of this signal.
HRD#	I	HIP Read Enable. When low, data is loaded to HD7:0, which should be sampled at positive edge of this signal.
HWR#	I	HIP Write Enable. Data at HD7:0 is sampled at positive edge of this signal.
HD7:0	I/O	HIP Address/Data Bus. Multiplexed address lines and data lines.
Internal ADC Interface		
ADCAIN	I	ADC Analog Input. Analog input spans between ADCREFP and ADCREFN.
ADCREFP	I	ADC Internal Reference Top Bias. Connect this pin to voltage between ADCVDDA and 2.0V.
ADCREFN	I	ADC Internal Reference Bottom Bias. Connect this pin to ground.
ADCVDDA	PWR	ADC Supply Voltage for Analog Circuit. Connect this pin to the +2.7V supply voltage.
ADCVSSA	GND	ADC Ground for Analog Circuit. Connect this pin to ground.

ADCVDDD	PWR	ADC Supply Voltage for Digital Circuit. Connect this pin to the +2.7V supply voltage.
ADCVSSD	GND	ADC Ground for Digital Circuit. Connect this pin to ground.
External DAC Interface		
DACMSCK	O	DAC Master Clock. $384 \times F_s$ clock.
DACBCK	O	DAC Bit Clock. $32 \times F_s$ or $64 \times F_s$ clock.
DACLRCK	O	DAC Sample Rate Clock. F_s clock.
DACSDATA	O	DAC Serial Data. Serial data.
DACDEEM	O	DAC Deemphasis. When deemphasis is on, this signal is high. It can be set/clear through HIP commands.
DACMUTE#	O	DAC Mute. Analog output mute. When external DAC is set to mute on, this signal is low. It can be set/clear through HIP commands.
Internal DAC Interface		
AOUTL	O	Analog Output for Left-Channel.
AOUTR	O	Analog Output for Right-Channel.
DACVHALF	I/O	DAC Reference Voltage Output for Bypass.
DACVREF	I/O	DAC Reference Voltage Output for Bypass.
DACVDDA	PWR	DAC Supply Voltage for Analog Circuit. Connect this pin to the +2.7V supply voltage.
DACVSSA	GND	DAC Ground for Analog Circuit. Connect this pin to ground.
Test Pins		
TESTSEL[2:0]	PWR	Test Mode. During normal operation, these pins should be tied to ground.
TESTOUT[1:0]	GND	Test Out. During normal operation, these pins need not be connected.
SCANEN	PWR	Scan Enable. During normal operation, these pins should be tied to ground.
Power/Ground Pins		
VDD	PWR	Supply Voltage. Connect this pin to the +2.7V supply voltage.
VSS	GND	Circuit Ground. Connect this pin to ground.
VDDIO	PWR	Supply Voltage for I/O Buffers. Connect this pin to the +2.7V supply voltage.
VSSIO	GND	Circuit Ground for I/O Buffers. Connect this pin to ground.

FUNCTIONAL DESCRIPTION

RESET/CLOCK UNIT

A single clock at the frequency of 16.9344MHz drives TL7232MD. The clock can be derived from an external source or from an industry standard crystal oscillator, generating input frequency of 16.9344MHz. The clock generation unit has a PLL, and all the internal clock signals including internal DAC/ADC clocks are generated with the input clock.

When TL7232MD is in power-on-reset, RESET signal should be active at least 150 μ s till the internal PLL is stabilized. To reset TL7232MD during normal operation, RESET signal should be active at least 16 cycles.

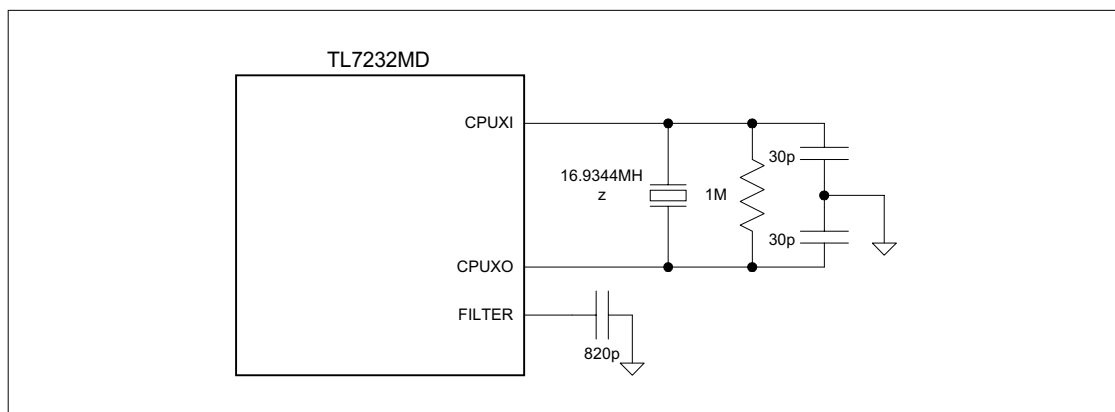


Figure 3. Clock Circuit

DSP CORE LOGIC

The core logic of TL7232MD is a 32-bit floating-point DSP processor. The independent multiplier and accumulator of TL7232MD can achieve high performance. Internal registers are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. Since all the data input/output transactions are managed by DMA, there is no computational overhead due to data transactions.

SERIAL INTERFACE

The serial interface of TL7232MD is used to receive MPEG bit stream data or transmit/receive voice data. It is configured to transfer 8 bits of data per word. It can be configured to be LSB-first or MSB first transfer mode. LSB-first means that the data bits are transmitted and received least-significant bit (LSB) first. MSB-first means that the data bits are transmitted and received most-significant bit (MSB) first. The clock for the serial interface should be generated externally.

The related signals are CLKXRM, DXRM, and REQSTRM. REQSTRM is used for synchronization between microcontroller and TL7232MD, and data is transferred during

REQSTRM active.

When microcontroller tries to send data to TL7232MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to transmit mode and send serial clock and serial data. After transmitting each byte, microcontroller should check REQSTRM to decide whether next byte is to be transmitted or not.

When microcontroller tries to receive data from TL7232MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to receive mode and send serial clock and receive serial data from TL7232MD. After receiving each byte, microcontroller should check REQSTRM to decide whether TL7232MD will transmit next byte or not.

HOST INTERFACE PORT (HIP)

Host interface port is used to send commands to and receive status information from TL7232MD. HIP of TL7232MD is a parallel I/O port that makes a connection to a host processor easily. Through the HIP, TL7232MD can be used as a memory-mapped peripheral to a host processor. The HIP can be thought of as an area of dual-port memory that allows communication between the computational core of the TL7232MD and host. The HIP is completely asynchronous. The host processor can write data into the HIP while the TL7232MD is operating at full speed. HIP transfers are managed using interrupt scheme.

HIP contains 21 registers. Four of them are data-in registers (HDI0/HDI1/HDI2/HDI3) and one of them is a status register (HSR4). The remaining 16 registers are data-out registers (HDO0/.../HDO15). Data written into HDIs by host are read by TL7232MD. Through these registers host can give necessary commands to TL7232MD. A command is written into a HDI0, and the required parameters of the command are written into the HDI1/HDI2/HDI3. The status register (HSR4) keeps the information whether data written into the data-in registers are read by TL7232MD. The status register is managed automatically by TL7232MD and can be read by host. TL7232MD starts HIP command processing when HDI0 register is written. So if a command requires parameters, user should write parameters first, and then write the command.

Serial ID number can be used to check whether any given command has been accepted or not. The serial ID number sent with a command to TL7232MD can be read from HDO0 when TL7232MD is processing the given command. Thus when a command is given to TL7232MD with a serial ID number, by reading HDO0 it can be examined that the command is being processed. Serial ID number itself hasn't any special meaning. If this feature is not needed, it is not required to send ID numbers with commands. Then the value of HDO0 is undetermined. There are exceptions for the ID number convention. If you use HIP command 0Dh (Revision Code), TL7232MD returns the TL7232MD revision number, not the ID number. For Sleep command (0Fh), you should not check ID number.

HDOs are written by TL7232MD and can be read by host. All HIP registers should be memory-mapped into the memory space of the host processor. The address space of those registers is shown in Table 4. The usable commands are listed in Table 6. The contents reported by HDOs are shown from Figure 4 to Figure 16.

Table 4. Address of Host Interface Port Registers

ADDRESS	REGISTERS	DESCRIPTION
0h	HDI0	Command
1h	HDI1	Serial ID Number
2h ~ 3h	HDI2/HDI3	Parameters if needed
4h	HSR4	Status Register (Fig. 4)
10h	HDO0	Command Serial ID Number (Fig. 5)
11h	HDO1	Decoder State (Fig. 6)
12h	HDO2	IO Status (Fig.7)
13h	HDO3	IO Status (Fig. 8)
14h	HDO4	Volume (Fig. 9)
15h	HDO5	Serial Interface Mode (Fig. 10)
16h ~ 1Fh	HDO6 ~ HDO15	The information provided by these registers depends on the mode setting of TL7232MD. (Refer to Table 5)

According to the reporting format mode of TL7232MD, the information provided by HDO6 to HDO15 has different meaning. (Refer to Table 5.) The reporting format mode can be set by using Report Format command (19h). For this command, refer to Table 6.

Table 5. The contents of HDO6 ~ HDO15 according to reporting format modes

ADDRESS	REGISTERS	DESCRIPTION
16h	HDO6	Mode0: 00h Mode1: Tone Control Status. When tone control is enabled, 1 is reported. Otherwise, 0 is reported. Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: Equalizer Control Status. When equalizer control is enabled, 1 is reported. Otherwise, 0 is reported.
17h	HDO7	Mode0: 00h Mode1: Tone Control - Prescaling Information Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control – Prescaling Information
18h	HDO8	Mode0: 00h Mode1: Tone Control – Bass Cutoff Frequency Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control – Band1 Gain
19h	HDO9	Mode0: 00h Mode1: Tone Control – Bass Gain Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control –Band2 Gain

1Ah	HDO10	Mode0: 00h Mode1: Tone Control – Treble Cutoff Frequency Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 12) Mode3: 00h Mode4: EQ Control – Band3 Gain
1Bh	HDO11	Mode0: 00h Mode1: Tone Control – Treble Gain Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 13) Mode3: 00h Mode4: EQ Control – Band4 Gain
1Ch	HDO12	Mode0: 00h Mode1: 00h Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 14) Mode3: 00h Mode4: EQ Control – Band5 Gain
1Dh	HDO13	Mode0: 00h Mode1: 00h Mode2: Bass Boost Information (Fig. 15) Mode3: 00h Mode4: EQ Control – Band6 Gain
1Eh	HDO14	Mode0: 00h Mode1: 00h Mode2: DAC Output Valid (Fig. 16) Mode3: 00h Mode4: 00h
1Fh	HDO15	Mode0: 00h Mode1: 00h Mode2: CRC Error Count Mode3: 00h Mode4: 00h

Table 6. Host Interface Port Commands

COMMAND	PARAMETER	MEANING	DESCRIPTION												
00h	None	Stop	Stop execution and go into WAIT state.												
01h	None	MP3 Decoding	Execute MP3 decoding.												
04h	None	Voice Encoding	Execute voice encoding (16Kbps).												
05h	None	Voice Decoding	Execute voice decoding (16Kbps).												
06h	None	Voice Encoding	Execute voice encoding (24Kbps).												
07h	None	Voice Decoding	Execute voice decoding (24Kbps).												
08h	None	Voice Encoding	Execute voice encoding (32Kbps).												
09h	None	Voice Decoding	Execute voice decoding (32Kbps).												
0Dh	None	Revision Code	Report the TL7232MD revision number in HDO0.												
0Fh	None	Sleep	Go into SLEEP state. This command should be used in WAIT state. If this command is used during algorithm execution, TL7232MD becomes unstable.												
10h	None	Mute ON	When using internal DAC, The output voltage level of AOUTL/AOUTR is GND. When using external DAC, DACMUTE# becomes active. After reset, mute is enabled												
11h	None	Mute OFF	Mute is disabled.												
14h	None	Internal DAC	Use internal DAC. After reset, TL7232MD is set to use internal DAC.												
15h	None	External DAC	Use external DAC. Internal DAC is disabled. The waveform of I/O pin related to external DAC is controlled according to External DAC Format or External DAC Format 2. After reset, TL7232MD is set to use internal DAC.												
16h	1byte	External DAC Format	Set the waveform of I/O pin related to external DAC. The parameter value of External DAC Format command should be as follows: {0, 0, 0, 0, BC64, I ² S, PL, PB}. For the meaning of BC64, I ² S, PL, and PB, refer to Figure 8.												
17h	None	MSB First	Serial Interface MSB-first mode. This is the default mode after reset.												
18h	None	LSB First	Serial Interface LSB-first mode												
19h	1byte	Report Format	The reported contents of HDO6 to HDO15 are changed according to parameter of this command. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Parameter</th> <th>Reporting Contents</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>all 00h</td> </tr> <tr> <td>1</td> <td>Tone Control Information</td> </tr> <tr> <td>2</td> <td>MP3 Decoding Information</td> </tr> <tr> <td>3</td> <td>Voice Encoding/Decoding Information</td> </tr> <tr> <td>4</td> <td>Equalizer Control Information</td> </tr> </tbody> </table>	Parameter	Reporting Contents	0	all 00h	1	Tone Control Information	2	MP3 Decoding Information	3	Voice Encoding/Decoding Information	4	Equalizer Control Information
Parameter	Reporting Contents														
0	all 00h														
1	Tone Control Information														
2	MP3 Decoding Information														
3	Voice Encoding/Decoding Information														
4	Equalizer Control Information														
1Ah	1byte	ADC/DAC Power Down Control	This command controls the power-down mode of internal ADC and DAC. The parameter value of this command should be as follows: {0, 0, 0, 0, 0, 0, ADCPD, DACPD}. For the meaning of ADCPD and DACPD, refer to Figure 8. After reset, internal ADC and DAC are active.												

1Bh	None	Voice Monitoring ON	During voice recording, the output of ADC is sent to DAC input. So, through DAC output you can monitor what is recorded. After reset, voice monitoring is disabled.
1Ch	None	Voice Monitoring OFF	This command makes that the output of ADC is not sent to DAC input. After reset, voice monitoring is disabled.
1Dh	1byte	Bit Stream Clock Polarity	This command controls the clock polarity of bit stream. The parameter value of command should be as follows: {0, 0, 0, 0, 0, 0, RXPOL, TXPOL}. For the meaning of RXPOL and TXPOL, refer to Figure 10.
20h	1byte	Bass Boost Control (MP3 Only)	Control Bass boost. The upper nibble of the parameter controls the cutoff frequency of bass boost, and the lower nibble controls the level of bass boost. The value of upper nibble should be in the range of 0 to 6. The cutoff frequency is $25 \times \text{upper nibble} + 50 \text{ (Hz)}$. If the values of the lower nibble is in the range of 0 to 12, the low frequency band below the cutoff frequency is boosted by 0dB ~ 18dB (1.5dB step). The other values mean no boost. For example, if the parameter value is 42h, then the cutoff frequency will be $25 \times 4 + 50 = 150\text{Hz}$, and the frequency band below 150Hz will be boosted by 3dB compared to the upper frequency band. In case of using bass boost, volume is reduced by $1.5 \times n \text{ dB}$ where n means the parameter value. The reset value is FFh(disabled).
21h	1byte	Volume Control	Control volume. The parameter should have the value of range from 0 to 255. If the value is n , the volume is attenuated by $n/2 \text{ dB}$ compared to maximum volume. The reset value is 0.
22h	1byte	Prescale Control	Control the prescaling. The parameter is a signed value and can be -128 to 127. The prescaling is done by $0.5 \times n \text{ dB}$ according to parameter value n . That is, 0h ~ 7Fh means 0dB ~ 63.5dB scaling, 80h ~ FFh means -64dB ~ -0.5dB scaling. The reset value is 0dB.
23h	1byte	Tone Control – Bass Gain (MP3 Only)	Control the Bass Gain. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n \text{ dB}$ according to parameter value n . The reset value is 0.
24h	1byte	Tone Control – Treble Gain (MP3 Only)	Control the Treble Gain. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n \text{ dB}$ according to parameter value n . The reset value is 0.
25h	1byte	Tone Control – Bass Cutoff (MP3 Only)	Control the Bass Cutoff Frequency. The parameter can have the value of 0 to 255. The cutoff frequency can be $20 + 5 \times n \text{ Hz}$ according to parameter value n . The reset value is 0.
26h	1byte	Tone Control – Treble Cutoff (MP3 Only)	Control the Treble Cutoff Frequency. The parameter can have the value of 0 to 255. The cutoff frequency can be $5000 + 20 \times n \text{ Hz}$ according to parameter value n . The reset value is 0.

27h	None	Tone Control – Enable (MP3 Only)	Enable the Tone Control Function. Tone Control Function is disabled when reset.
28h	None	Tone Control – Disable (MP3 Only)	Disable the Tone Control Function. Tone Control Function is disabled when reset.
30h	None	MP3 CRC Bypass (MP3 Only)	During MP3 decoding, even if the input bit stream contains the CRC field, TL7232MD doesn't check the CRC error. After reset, TL7232MD is set to check CRC error.
31h	None	MP3 CRC Check	During MP3 decoding, if the input bit stream contains the CRC field, check the CRC error. If an error occurs, TL7232MD outputs 0 during the period of corresponding MP3 frame. The reset value is MP3 CRC check.
40h	1byte	EQ Control – Band1 Gain (MP3 Only)	Control the gain of Band1(<30Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
41h	1byte	EQ Control – Band2 Gain (MP3 Only)	Control the gain of Band2(30Hz~125Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
42h	1byte	EQ Control – Band3 Gain (MP3 Only)	Control the gain of Band3(125Hz~500Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
43h	1byte	EQ Control – Band4 Gain (MP3 Only)	Control the gain of Band4(500Hz~2KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
44h	1byte	EQ Control – Band5 Gain (MP3 Only)	Control the gain of Band5(2KHz~8KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
45h	1byte	EQ Control – Band6 Gain (MP3 Only)	Control the gain of Band6(>8KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value n . The reset value is 0dB.
46h	None	EQ Control – Enable (MP3 Only)	Enable the Equalizer Function. The equalizer function is disabled after reset.
47h	None	EQ Control – Disable (MP3 Only)	Disable the Equalizer Function. The equalizer function is disabled after reset.
8xh	None	External DAC Format2	Same as External DAC Format command. Parameter values are located at lower nibble of the command. The command should be the form of {1, 0, 0, 0, BC64, I ² S, PL, PB}. Refer to Figure 8.

After reset, internal ADC and DAC are in active state. Internal ADC and DAC can go into power-down mode by using PWRDN pin or ADC/DAC power down control command (1Ah). For internal DAC, it is also in power-down mode if you enable external DAC. In controlling the power-down mode of DAC, it is recommended to use Mute On and Mute OFF commands (10h and 11h). That is, before internal DAC is made to be in power-down mode, Mute On command (10h) should be sent to TL7232MD. After you make the internal DAC active, it is recommended to keep mute-on state at least 150us, and then you may send Mute OFF command (11h) to TL7232MD.

Bass boost control command (20h) is another form of tone control command (23h ~28h). It is implemented by using the same filter as tone control command. Thus, if bass boost control command is received with valid parameter value, gains and cutoffs are changed as follows;

- Bass gain and cutoff frequency of tone control are changed according to the parameter value.
- Treble gain is changed to 0.
- Prescaling is set to -12dB to remove clipping noise.
- Tone control is enabled.

If bass boost command is received with invalid parameter value, the gains and cutoff frequencies are not changed, and tone control is disabled. If a command related to tone control is received, only the related gain or cutoff frequency is changed, and the command has no effect on the tone control enable/disable and prescaling, and the information of bass boost which is reported through HDO13 is not changed. For the tone control enable command (27h), it just enables the tone control function, and has no effect on the gains and cutoff frequencies. Tone control disable command (28h) disables tone control function, and changes the bass boost status, which is reported through HDO13 to FFh (disable).

Prescaling has effect when tone control or equalizer is enabled or bass boost command is received.

Equalizer consists of 6 bands, and band1 and band6 are shelving type, band2 to band5 are peaking type. Since each band has relatively small Q value, correction matrix is automatically used to complement this small Q value whenever attenuation value is set by using EQ gain control commands (40h ~ 45h). It is not recommended that gain difference of neighbor bands exceed 10dB.

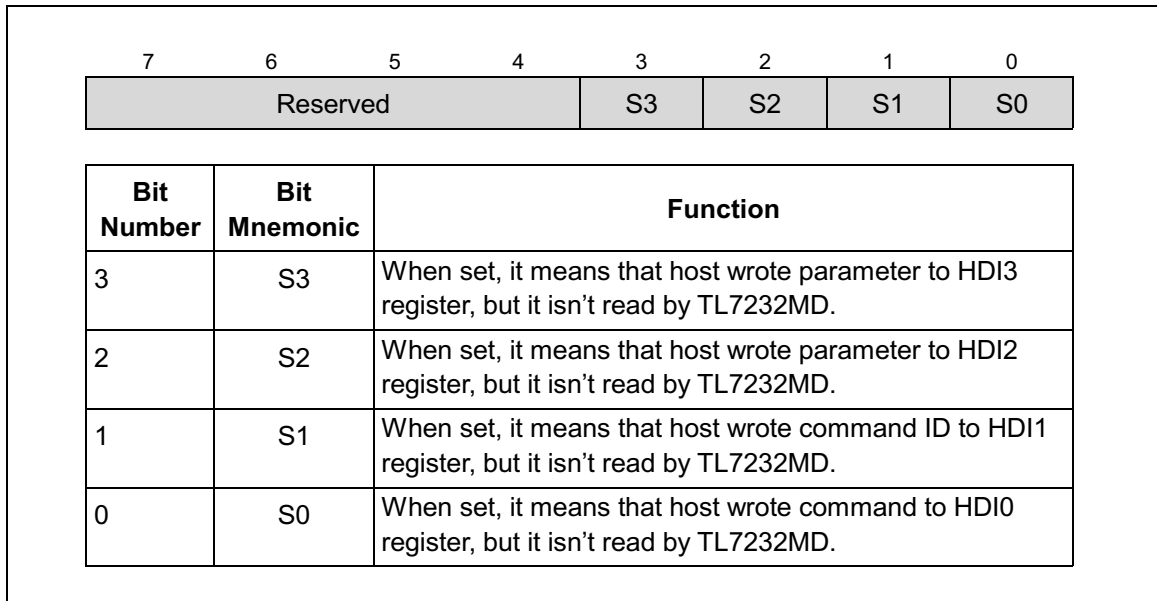


Figure 4. HDI Status Reported through HSR4

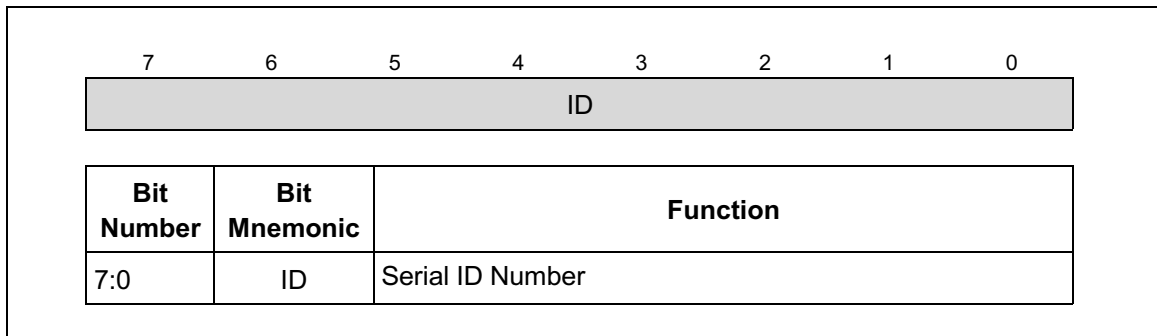


Figure 5. Command ID reported through HDO0

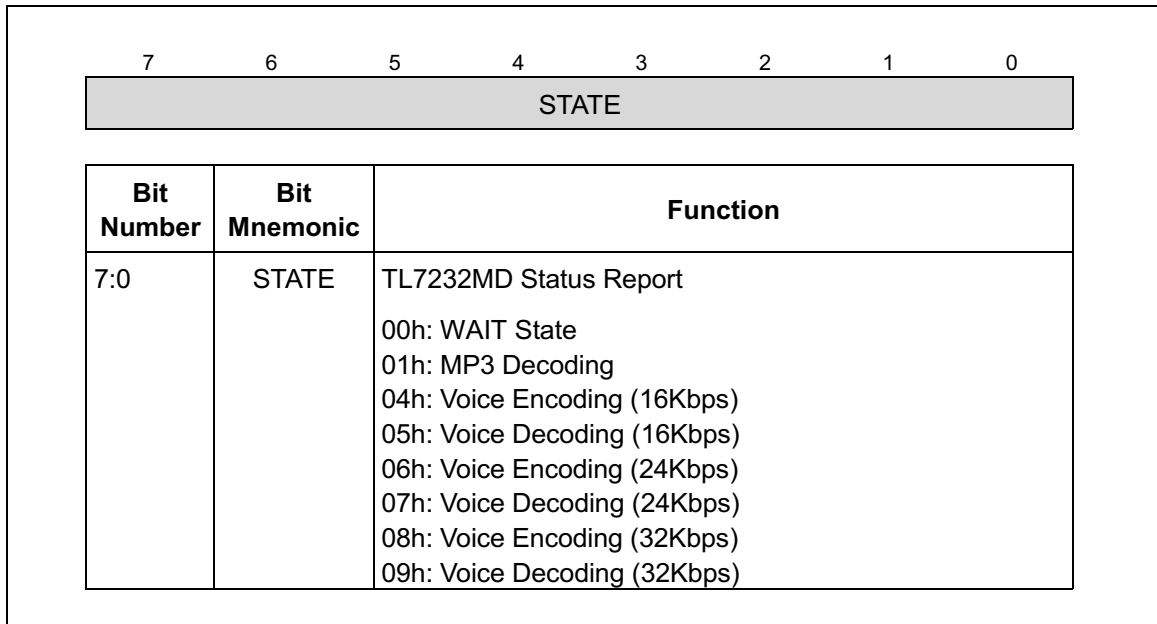


Figure 6. TL7232MD Status reported through HDO1

	7	6	5	4	3	2	1	0
	VMON	Reserved			DE	MU#	SF	

Bit Number	Bit Mnemonic	Function
7	VMON	Voice Monitoring Status: When set, voice monitoring is enabled. Reset value is 0.
3	DE	Deemphasis Enable: When set, deemphasis is enabled. Reset value is 0.
2	MU#	Mute Enable: When cleared, mute is on. Reset value is 0.
1:0	FS	Sampling Frequency: It shows the sampling frequency of bit stream. 00: 44.1KHz DAC / No ADC 01: 48KHz DAC / No ADC 10: 32KHz DAC / No ADC 11: No DAC / 8KHz ADC (Voice Monitoring Disabled) 11: 32KHz DAC / 8KHz ADC (Voice Monitoring Enabled) Reset value is 00.

Figure 7. I/O Status reported through HDO2

7	6	5	4	3	2	1	0
ADCPD	DACPD	BC64	I2S	PL	PB	EDAC	Reserved
Bit Number	Bit Mnemonic	Function					
7	ADCPD	ADC Power-down: When set, internal ADC is in power-down mode. When cleared, internal ADC is active. Reset value is 0.					
6	DACPD	DAC Power-down: When set, internal DAC is in power-down mode. When cleared, internal DAC is active. Reset value is 0.					
5	BC64	Bit Clock Select: When set, DACBCK is 64Fs. When cleared, DACBCK is 32Fs. <u>64Fs mode is valid when I²S mode is enabled.</u> Reset value is 0.					
4	I2S	I ² S Format Enable: When set, I ² S format (1 bit delay), When cleared normal PCM format. Reset value is 0.					
3	PL	Polarity of DACLRCK: When cleared, right channel data is sent through DACSDATA during LRCK=0. When set, right channel data is sent through DACSDATA during LRCK=1. Reset value is 0. (Refer Figure17.)					
2	PB	Polarity of DACBCK: When cleared, DACSDATA has valid data between falling edges of DACBCK. When set, DACSDATA has valid data between rising edges of DACBCK. (Refer Figure17.) Reset value is 0.					
1	EDAC	External DAC Enable: When set, external DAC is used. Reset value is 0.					

Figure 8. I/O Status reported through HDO3

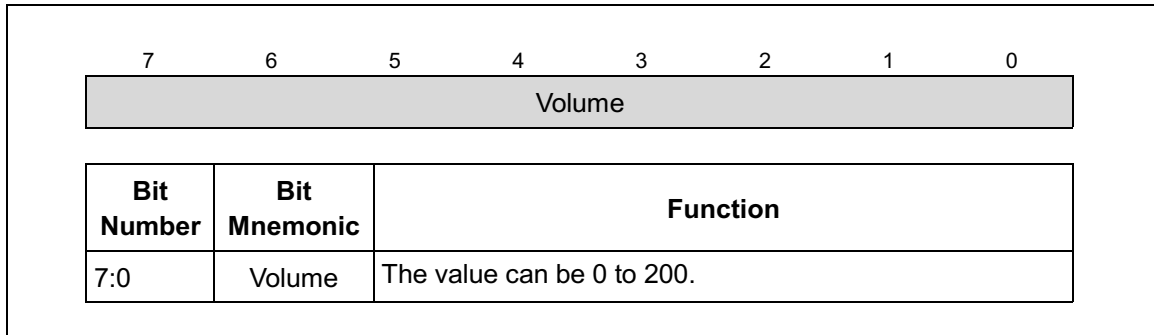


Figure 9. Volume reported through HDO4

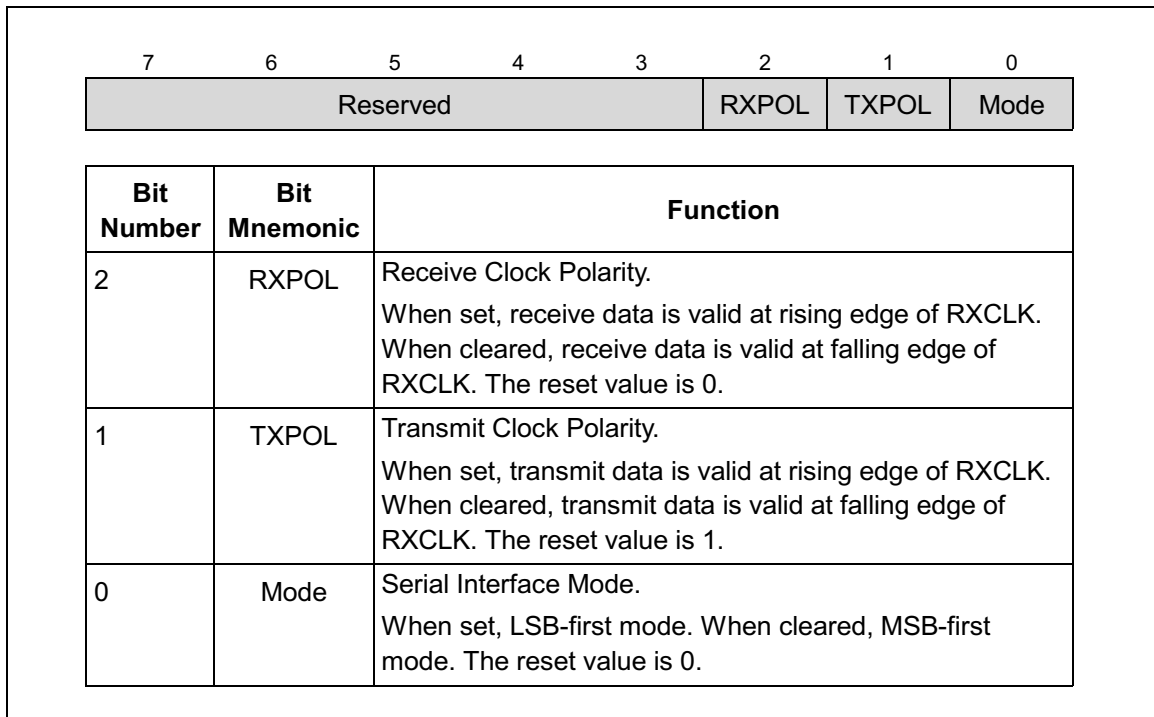


Figure 10. Serial Interface Mode reported through HDO5

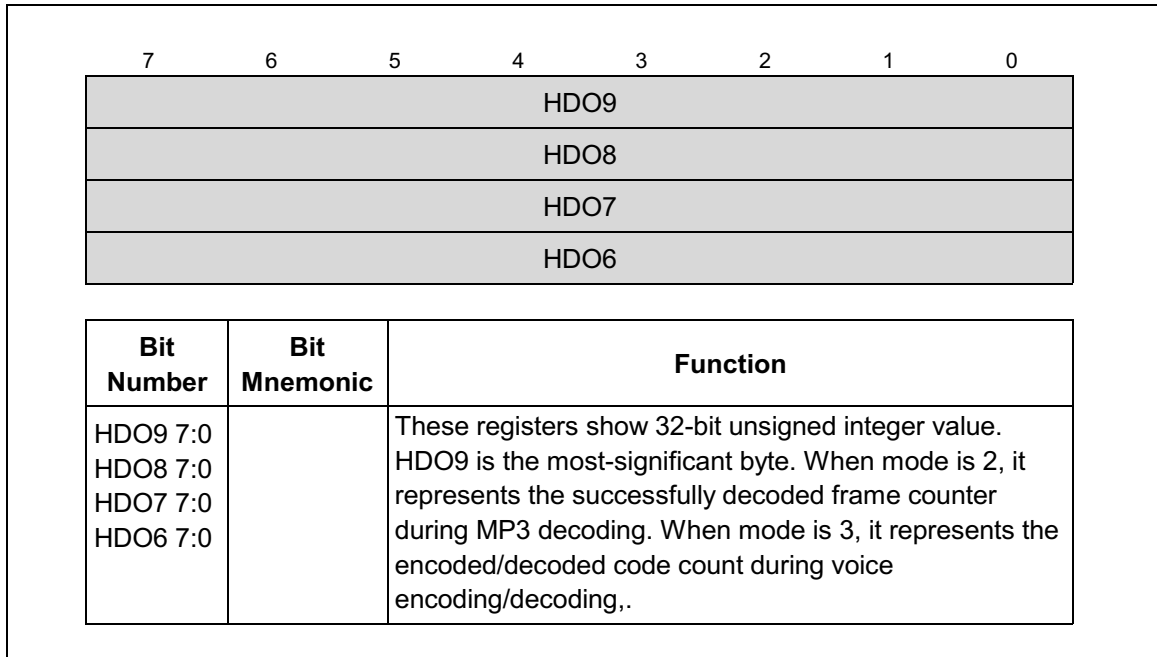


Figure 11. Count Value reported through HDO6 ~ HDO9

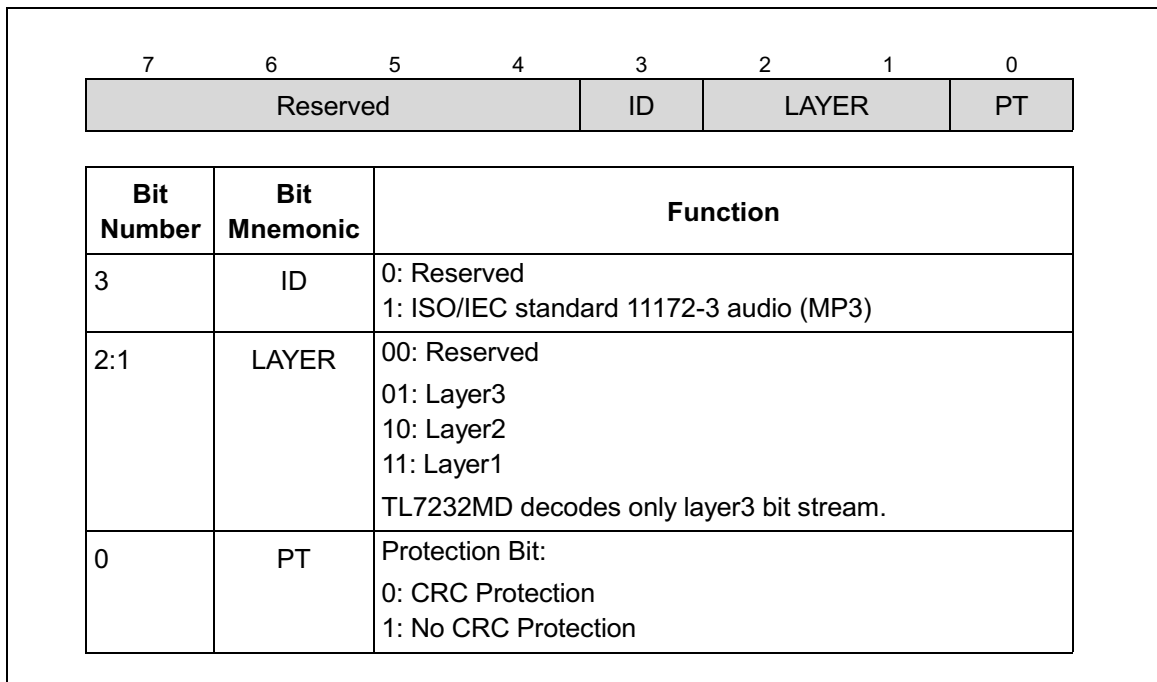


Figure 12. Frame Header reported through HDO10 when mode is 2.

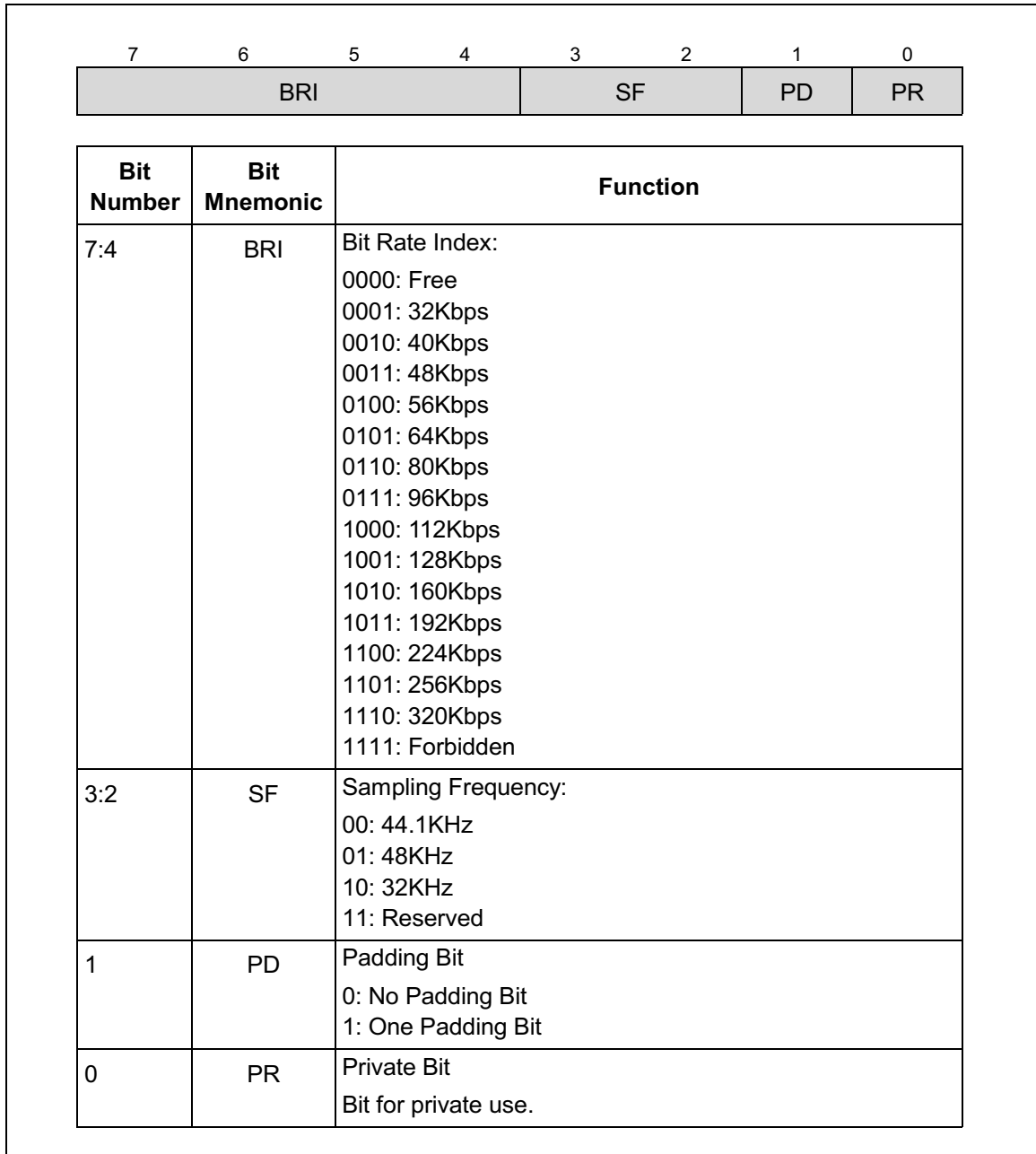


Figure 13. Frame Header reported through HDO11 when mode is 2.

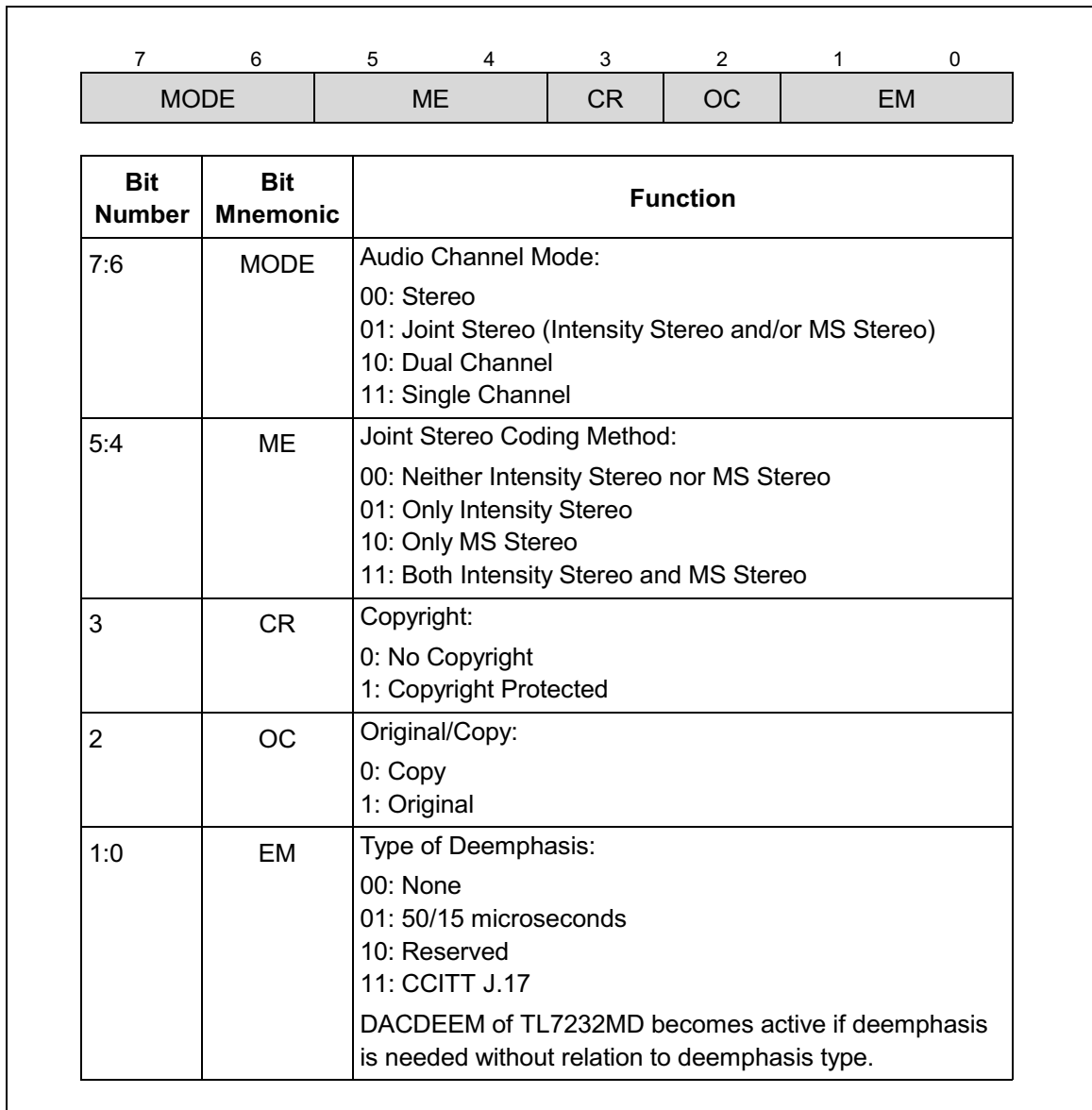


Figure 14. Frame Header reported through HDO12 when mode is 2.

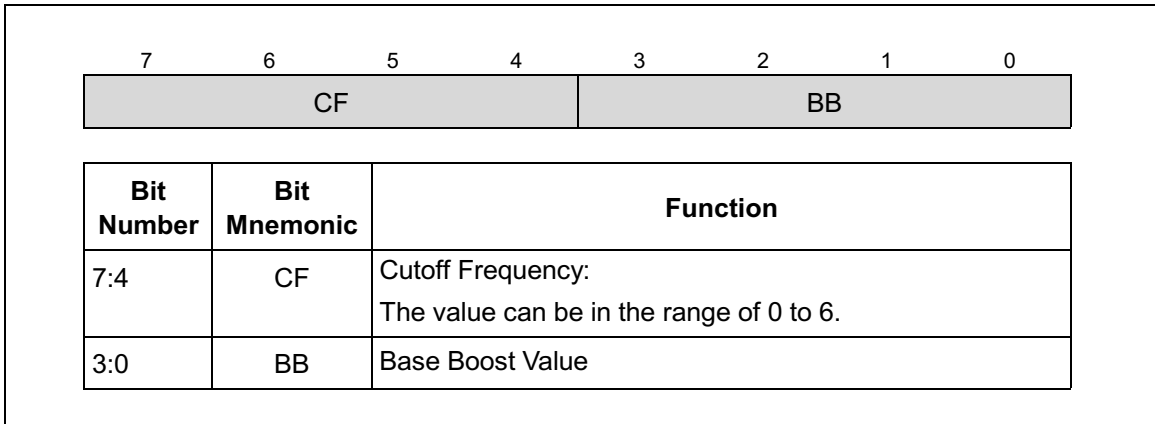


Figure 15. Bass Boost Information reported through HDO13 when mode is 2.

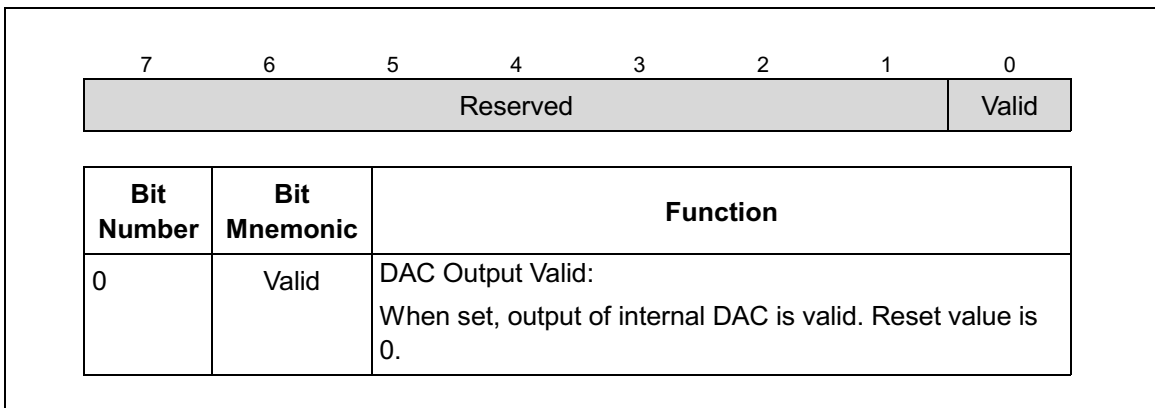


Figure 16. DAC Output Status reported through HDO14

DAC

DAC of TL7232MD employs the 1-bit 4th-order sigma-delta architecture with 16-bit resolution, over-sampling of 64X. Analog post-filter with low clock sensitivity and linear phase can filter out the shaping-noise and output analog voltage with high resolution. The characteristic of Internal DAC is shown Table 7.

Table 7. Characteristics of Internal DAC

PARAMETER	MIN	TYP	MAX	UNITS
Resolution		16		bits
SNR		79.7		dB
THD		84.9		dB
SNDR		78.5		dB
Reference Voltage Output (DACVREF)		0.5× DACVDDA		V
Frequency Response		± 0.1	± 0.5	dB
Analog Output				
Voltage Range		0.5× DACVDDA		V _{pp}
Load Impedance	10K			Ω
Digital Filter				
Pass Band Ripple		± 0.0072		dB
Stop and Attenuation		62.7		dB
Pass Band		0.45		F _s

(DACVDDD/DACVDDA=2.7V, Temp=25°C, F_s=44.1KHz, Signal Freq.=20~20KHz, C_{load} of AOUTL/AOUTR = 10pF)

With TL7232MD, user can configure whether the internal DAC is used or not. The configuration of DAC can be achieved through HIP commands shown in Table 5. When using internal DAC, the following circuit in Figure 17 is recommended.

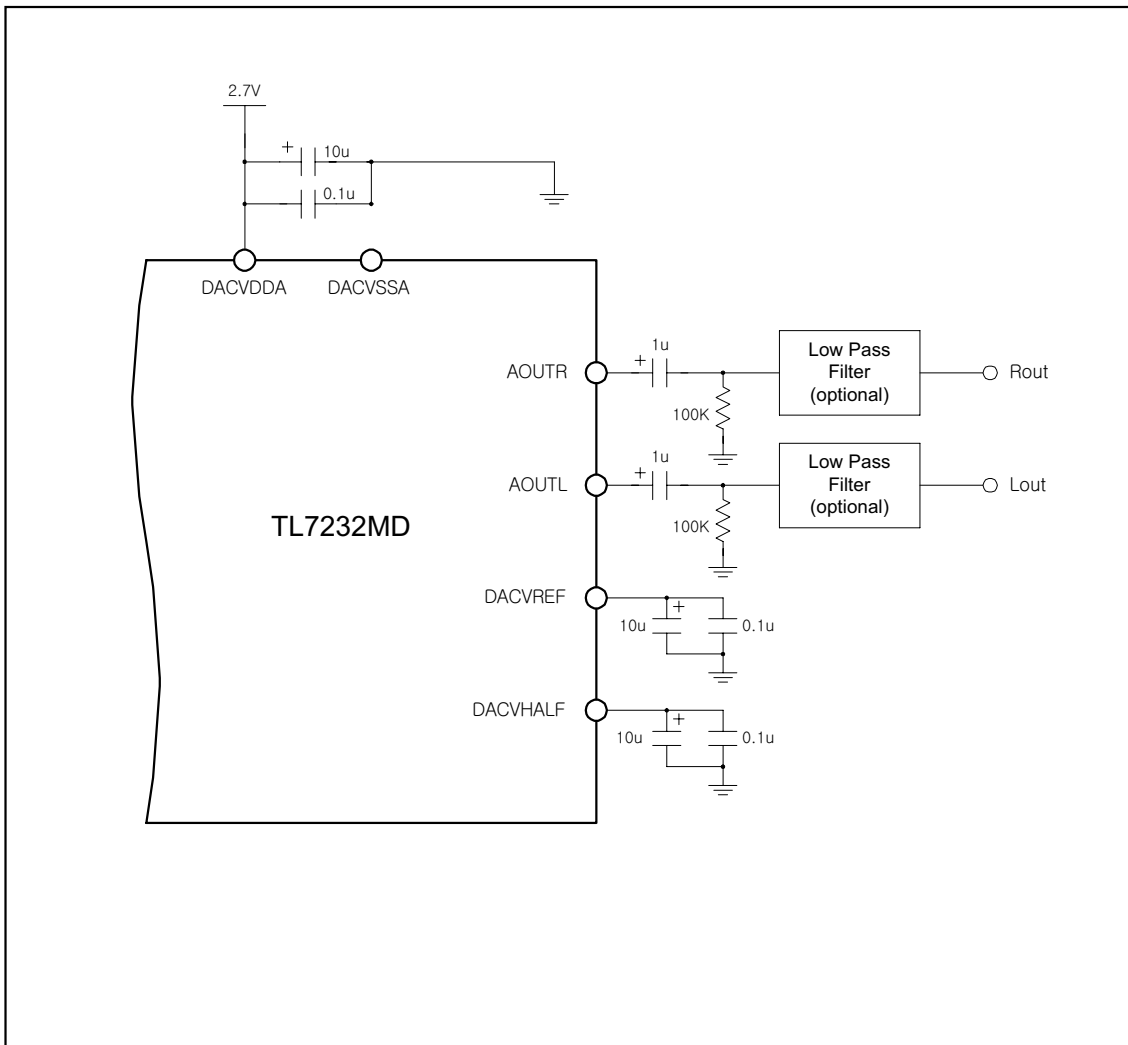


Figure 17. Reference Circuit when using internal DAC

External DAC Interfaces

TL7232MD supports twelve external interface formats. Four of them, for example, are shown in Figure 18. The interface can be configured through HIP commands. The frequency of DACBCLK is 32/64 times of that of DACLRCK. When voice signal is recorded or reproduced, only 32KHz of DACLRCK is used.

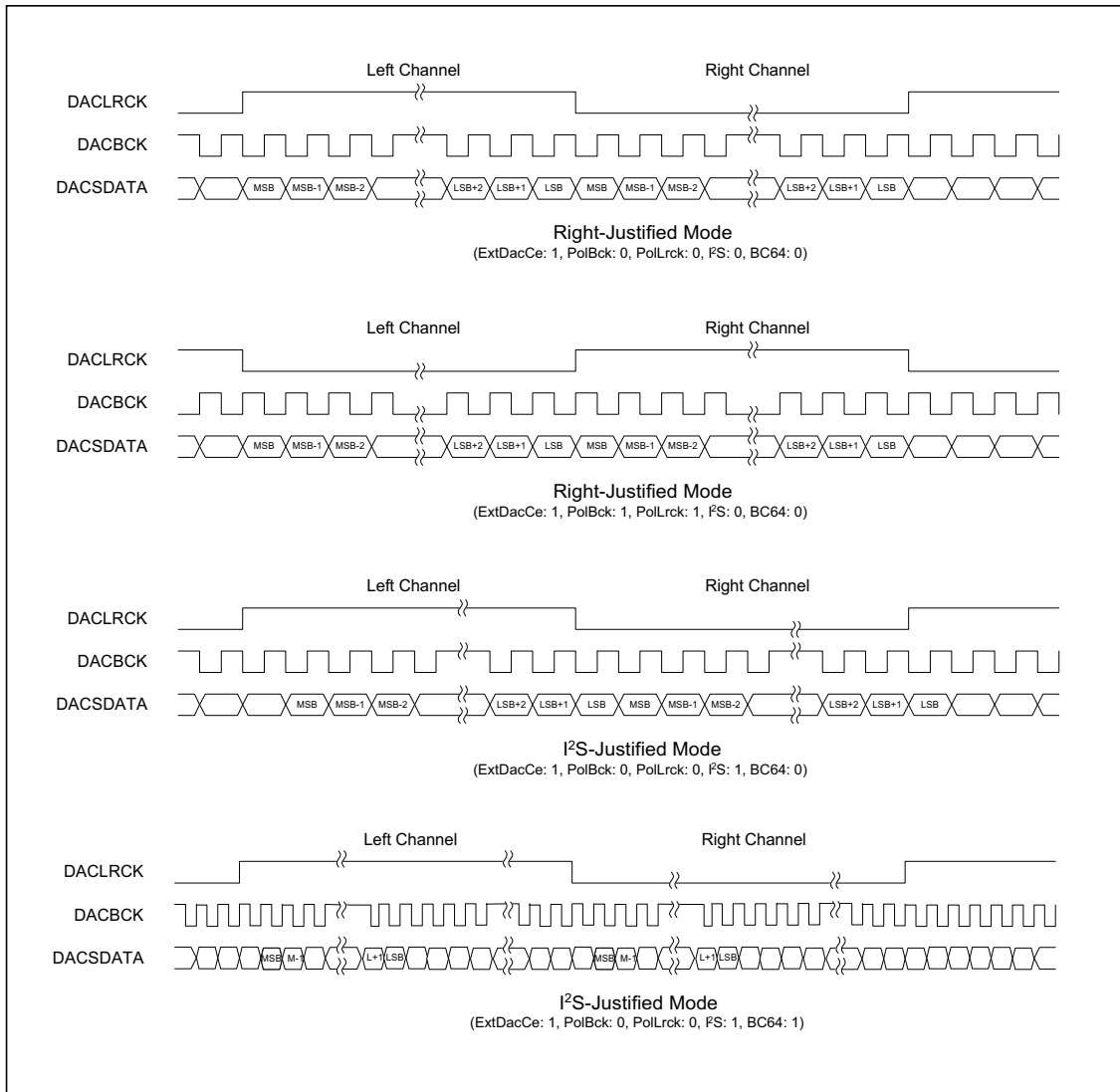


Figure 18. Examples of External DAC Interfaces

ADC

The internal ADC of TL7232MD is 12-bit resolution ADC. It is recycling type ADC with sample-and-hold function. The analog input ADCAIN should be single-ended type with the range from ADCREFP to ADCREFN. This ADCAIN voltage follows reference voltage range fundamentally. So, if user wants to alter the input range, the voltage value of ADCREFP should be changed. But ADCREFP should be greater than 2.0V. The characteristic of Internal ADC is shown Table 8.

Table 8. Characteristics of Internal ADC

PARAMETER	MIN	TYP	MAX	UNITS
THD		74.3		dB
SNR		64.9		dB
SNDR		64.4		dB

(ADCVDDD/ADCVDDA=2.7V, ADCAIN=8KHz)

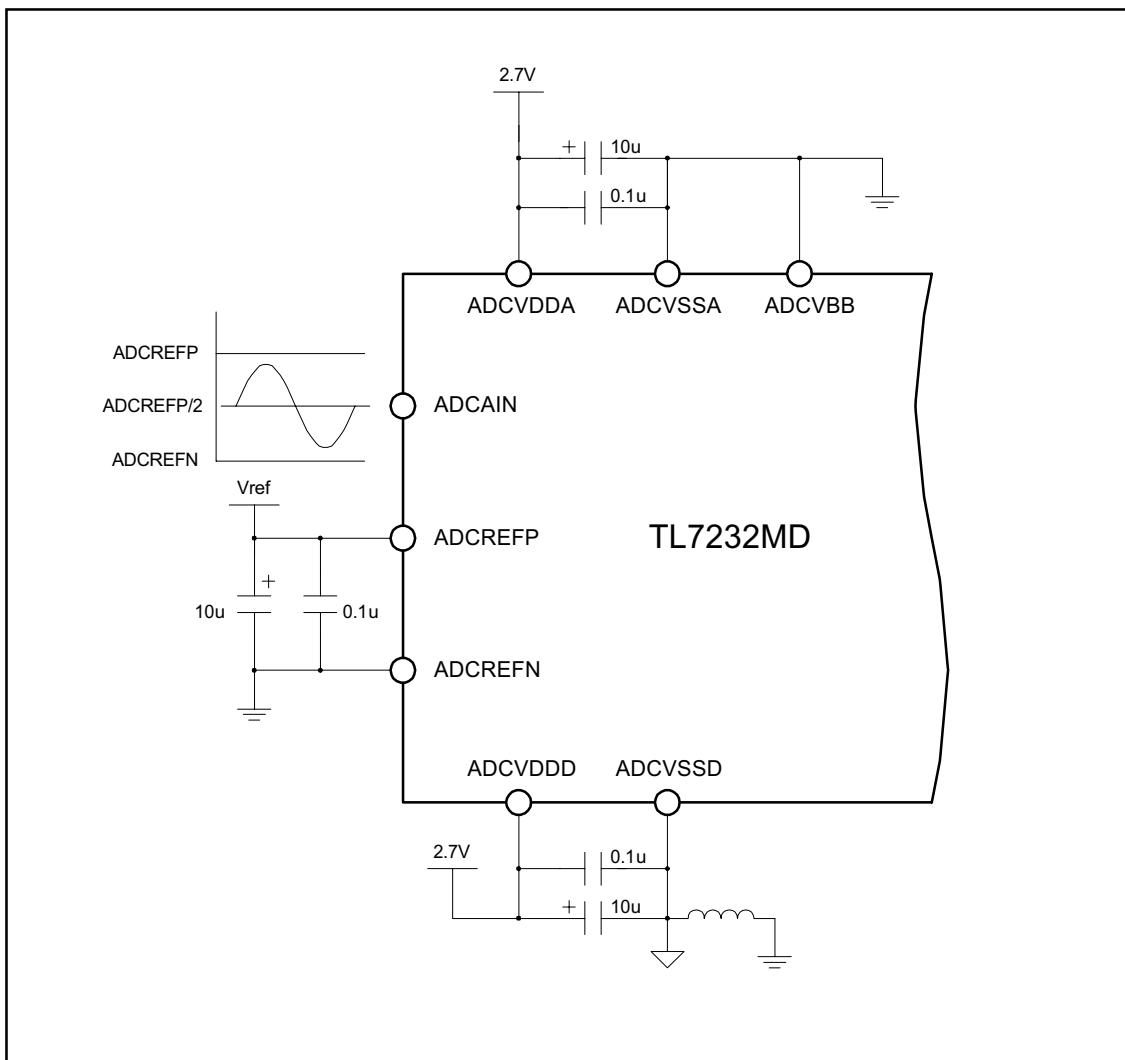


Figure 19. Reference Circuit when using internal ADC

With TL7232MD, the circuit in Figure 19 is recommended to use internal ADC.

Voice Record/Playback Function

TL7232MD records voice data from ADC in 8kHz sampling rate. There are three compression modes according to bit rates of compressed data: high quality (32Kbps), medium quality (24Kbps) and low quality (16Kbps). In high quality mode, relatively large bits are allocated for compressed data to achieve high quality of the sound. In low quality mode, smaller bits are allocated to record much more samples in the same size of storage media. Medium quality mode gives tradeoff between high and low quality modes. Compressed codes are byte-aligned and transmitted to host MCU through the serial port.

When voice signal is recorded, you can monitor (or hear) the sound. By using Voice Monitoring ON (1Bh) command, you can make the monitoring be enabled. The output of internal ADC is interpolated and passed to the input of internal DAC. When voice monitoring is enabled, volume can be controlled by Volume Control (21h) command. By using Voice Monitoring OFF (1Ch) command, you can make the monitoring be disabled.

In playback the codes are uncompressed to PCM samples, with the compression mode in recording, and then oversampled to 32 kHz and output to DAC. Compressed codes are transmitted from host MCU through the serial interface.

Table 9 is the summary of the relation between compression modes and code size.

Table 9. Summary of Three Voice Compression Modes

COMPRESSION MODES	CODE LENGTH (BIT)	RECORDING TIME FOR 32MB STORAGE MEDIA
High Quality (32Kbps)	4	140 min.
Medium Quality (24Kbps)	3	186 min.
Low Quality (16Kbps)	2	280 min.

Lower Power Operation

TL7232MD has low-power feature that makes the processor get into very low-power dormant states through hardware or software control. The power saving scheme is explained with the state diagram of TL7232MD shown in Figure 20.

RUN

In this state, TL7232MD decodes MP3 or compressed voice bit stream, or encodes voice signal. Also in this state it can process other HIP commands such as 20h and 21h. HIP command 01h, 04h through 09h, and 0Fh should not be used in this state. TL7232MD consumes normal power at this state, it processes all internal functions and drives external pads. It can transit to WAIT state with HIP command 00h. When there is no job left or it waits available data, power consumption is reduced as that of WAIT state.

WAIT

When RESET signal becomes active, TL7232MD goes into WAIT state. There it can transit to RUN, or SLEEP state. When TL7232MD is in this state, it is ready to receive any HIP commands from host. It can go into RUN state when it receives HIP commands such as 01h, 04h though 09h. Also it can process other HIP commands such as volume control (21h) etc. in this state. TL7232MD goes into this state through HIP command 00h from RUN state. When TL7232MD is in this state, only peripheral interface block consumes power. That is, internally generated peripheral clock is active but clock for the DSP core logic is not. When it receives HIP command 0Fh, it goes into SLEEP state in which more power is saved.

SLEEP

In SLEEP state, only internal analog blocks such as PLL, ADC and DAC of TL7232MD consume power. In this state, internal ADC and DAC are disabled. But PLL consumes normal operation power. In this state, TL7232MD can transit to PWRDOWN state when external PWRDN pin becomes active. Active WAKEUP signal changes its state from SLEEP to WAIT.

PWRDOWN

When TL7232MD is in SLEEP state and PWRDN signal becomes active, it transits to PWRDOWN. To make TL7232MD stay in this state, the external PWRDN signal keeps its active state. When the PWRDN signal becomes inactive, TL7232MD exits from this PWRDOWN state, and then goes into SLEEP state. When it changes its state from PWRDOWN to SLEEP, this state should not be changed during minimum 150 μ s until internal PLL is stabilized. TL7232MD consumes the minimum power at this state because all internal logic blocks and analog blocks are power-downed.

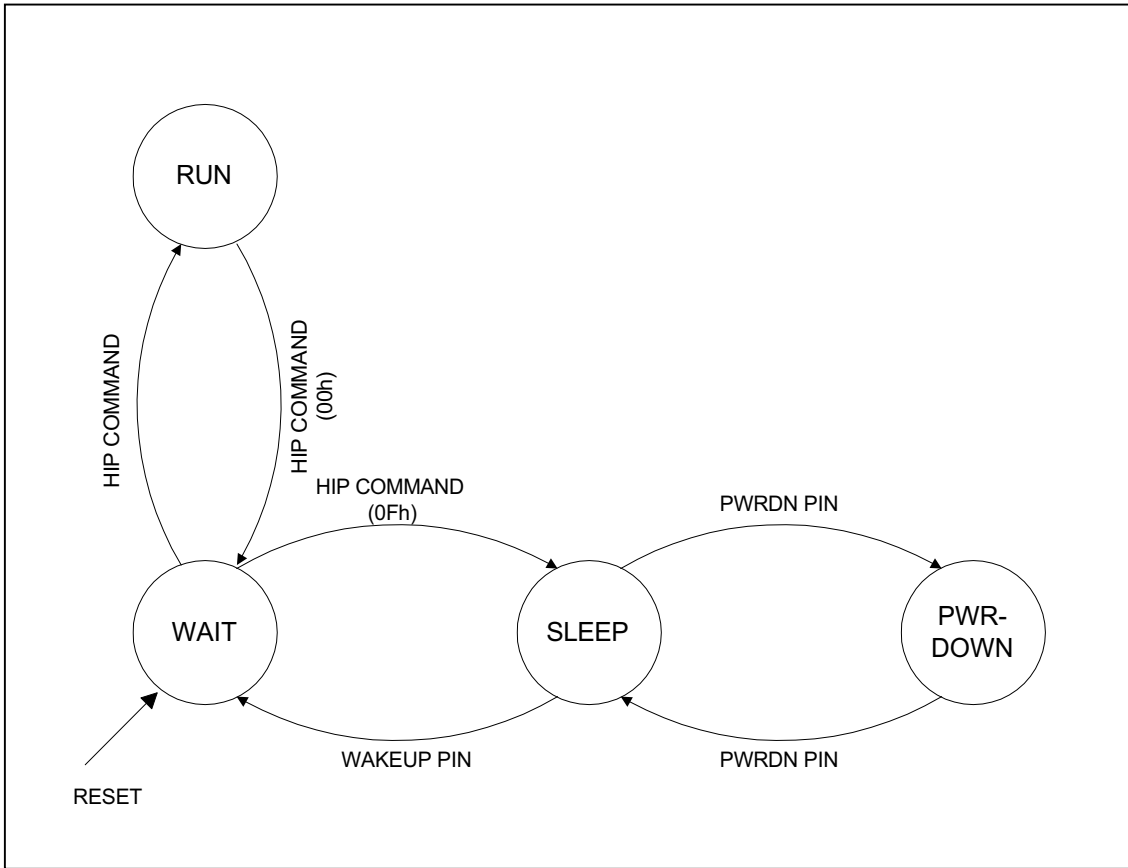


Figure 20. Decoder States and Power Management

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (See Notes)†

Symbol	Parameter	Rating	Unit
V_{DD}	DC Supply Voltage	-0.3 to 3.8	V
V_{IN}	DC Input Voltage	-0.3 to 5.5	V
I_{IN}	DC Input Current	± 10	mA
T_{STG}	Storage Temperature	-40 to 125	$^{\circ}\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “DC ELECTRICAL CHARACTERISTICS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

NOTE 2: This value was obtained under specially produced worst-case test conditions for the TL7232MD, which are not sustained during normal device operation.

DC ELECTRICAL CHARACTERISTICS (Note3)†

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	2.4	2.7	3.0	V
V_{SS}	Supply voltage		0		V
V_{IH}	High level input voltage	1.8		$V_{DD} + 0.3$	V
V_{IL}	Low level input voltage	-0.3		0.6	V
V_{OH}	High level output voltage	2			V
V_{OL}	Low level output voltage			0.4	V
I_{IH}	High level input leakage current without internal pull-up	-10		+10	μA
I_{IL}	Low level input leakage current without internal pull-up	-10		+10	μA
I_{RN}	Supply current in RUN state	48			mA
I_{WT}	Supply current in WAIT state	20			mA
I_{SL}	Supply current in SLEEP	6			mA
I_{PD}	Supply current in PWRDOWN state	250			μA
C_{IN}	Input capacitance			4	pF
C_{OUT}	Output capacitance			4	pF
T_A	Air temperature	-40		85	$^{\circ}\text{C}$
V_{CPUXI}	High level input voltage for CPUXI	2.5		$V_{DD} + 0.3$	V

† For TL7232MD, all typical values are at $V_{DD} = 2.7\text{ V}$, T_A (air temperature) = 25°C .

NOTE 3: All voltage values are with respect to V_{SS} . All input and output voltage levels are TTL-compatible. CLKIN can be driven by CMOS clock.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

AC ELECTRICAL CHARACTERISTICS

AC Test Condition

Parameter	Value
Temperature	85°C
Supply Voltage	2.7V
Input Rise and Fall Times	2ns
Output Load	10pF

Serial port

The following table defines the timing parameters for the serial port pins. The numbers shown in Figure 21 ~ Figure 23 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
1	T_{CC}	Cycle time of CLKXRM	144.7		ns
2	T_D	Delay time, CLKXRM to DXRM valid	42.2	78.4	ns
3	T_{SU}	Setup time, DXRM before CLKXRM low	1.9		ns
4	T_H	Hold time, DXRM from CLKXRM low	1.2		ns
5	T_{REQ}	Request check time, falling edge of CLKXRM to falling edge of REQSTRM	295.2	331.3	ns

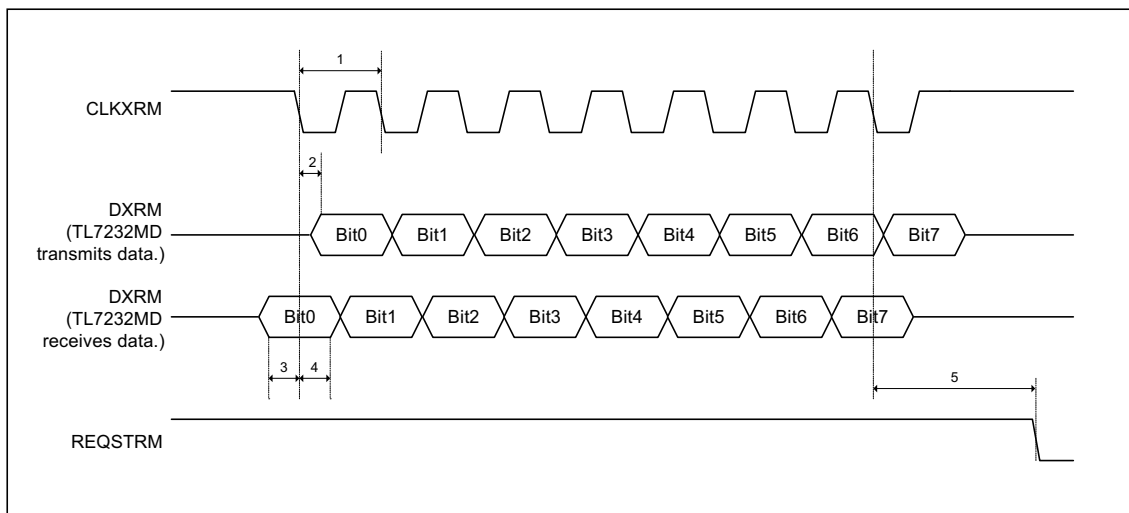


Figure 21. Timing for Serial Port in case of LSB-First Mode
(When RXPOL = 0, TXPOL = 1)

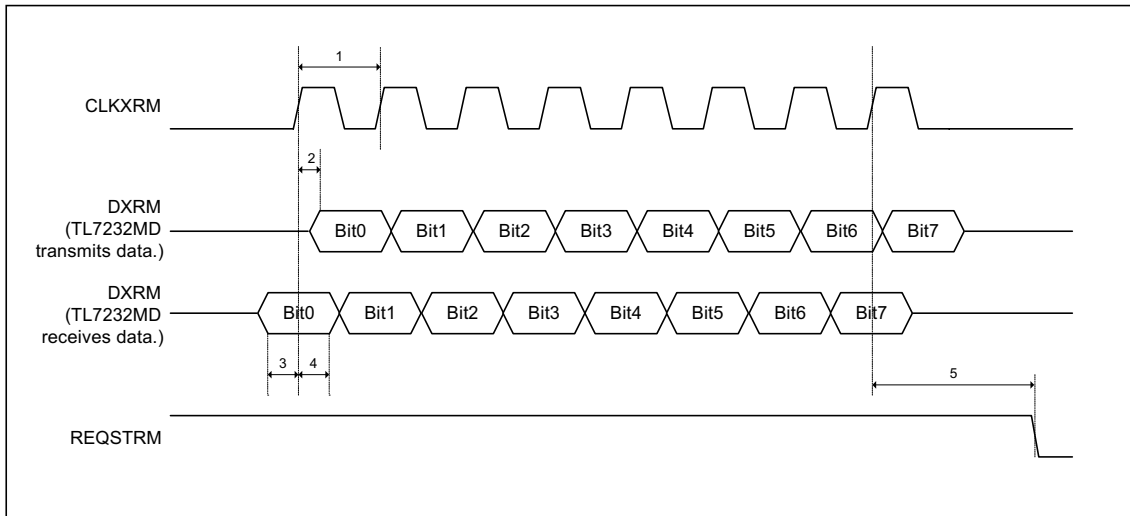


Figure 22. Timing for Serial Port in case of LSB-First Mode
(When RXPOL = 1, TXPOL = 0)

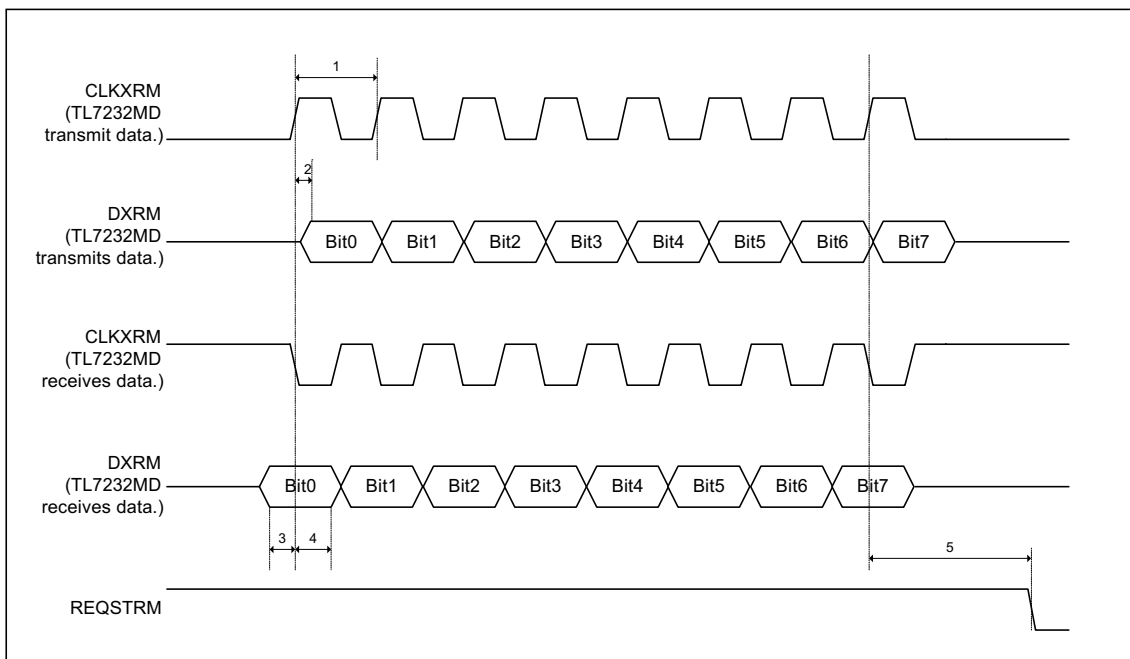


Figure 23. Timing for Serial Port in case of LSB-First Mode
(When RXPOL = 0, TXPOL = 0)

Host interface Port

The following table defines the timing parameters for the Host Interface Port I/O pins. The numbers shown in Figure 24 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
6	T_{HAW}	HALE pulse width	2.0		ns
7	T_{HDSU}	Setup time, HD address setup before HALE low	2.0		ns
8	T_{HDH}	Hold time, HD address hold after HALE low	0.8		ns
9	T_{HAS}	Start of write or read after HALE low	0.0		ns
10	T_{HDSU}	Setup time, HD data setup before end of write	0.7		ns
11	T_{HDH}	Hold time, HD data hold after end of write	2.2		ns
12	T_{HRW}	Read or write pulse width	36.2		ns
13	T_{HDE}	HD data enabled after start of read	7.8		ns
14	T_{HDD}	HD data valid after start of read	7.9		ns
15	T_{HRDH}	HD data hold after end of read	3.7	7.8	ns
16	T_{HRDD}	HD data disabled after end of read	4.2	7.9	ns

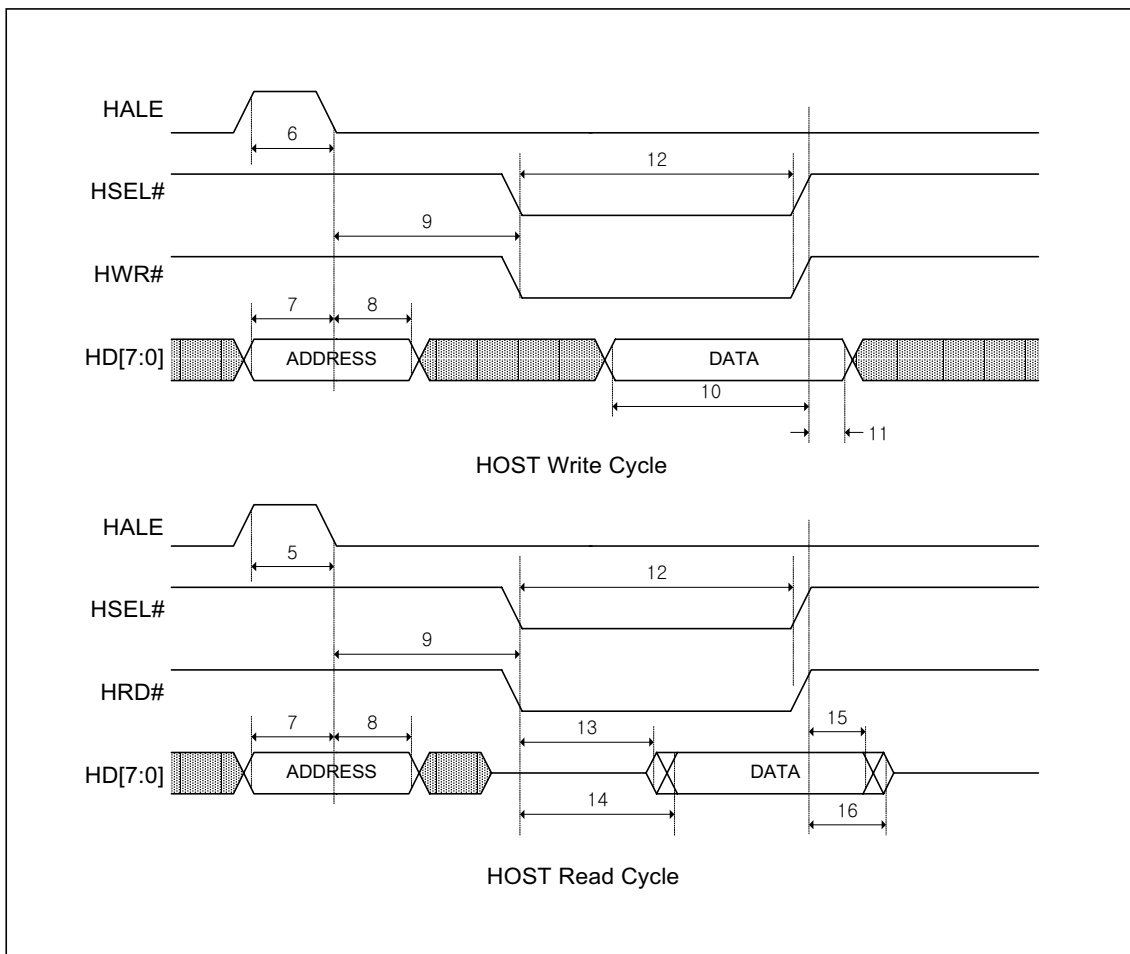
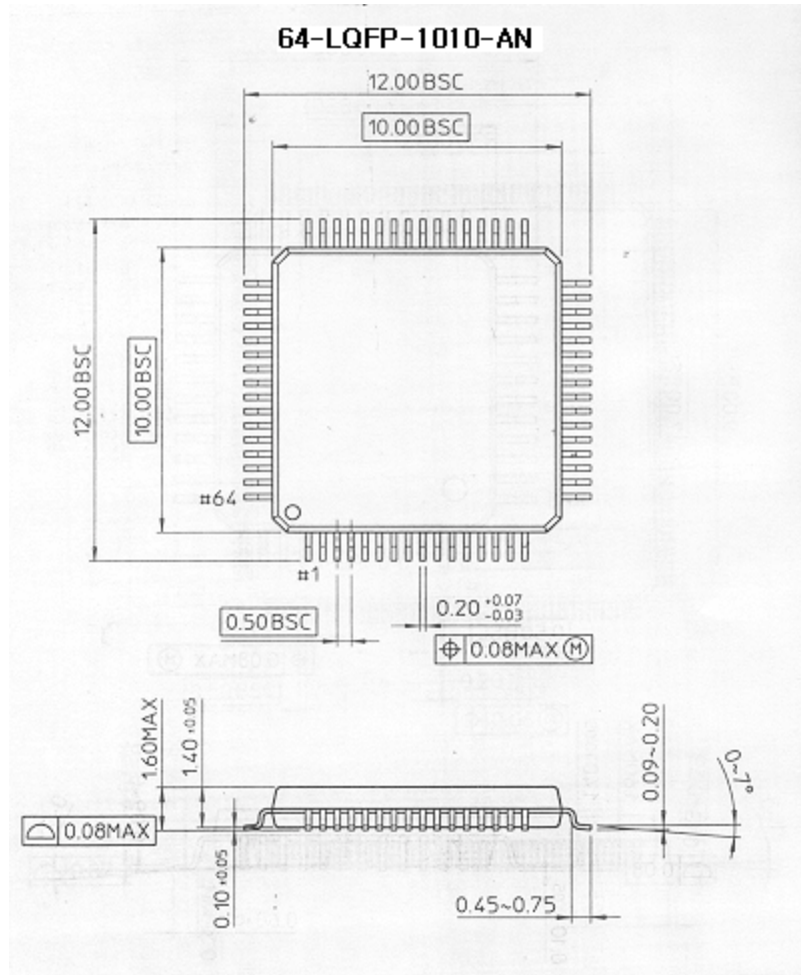


Figure 24. Timing for Host Interface Port pins

PACKAGE DIMENSION



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